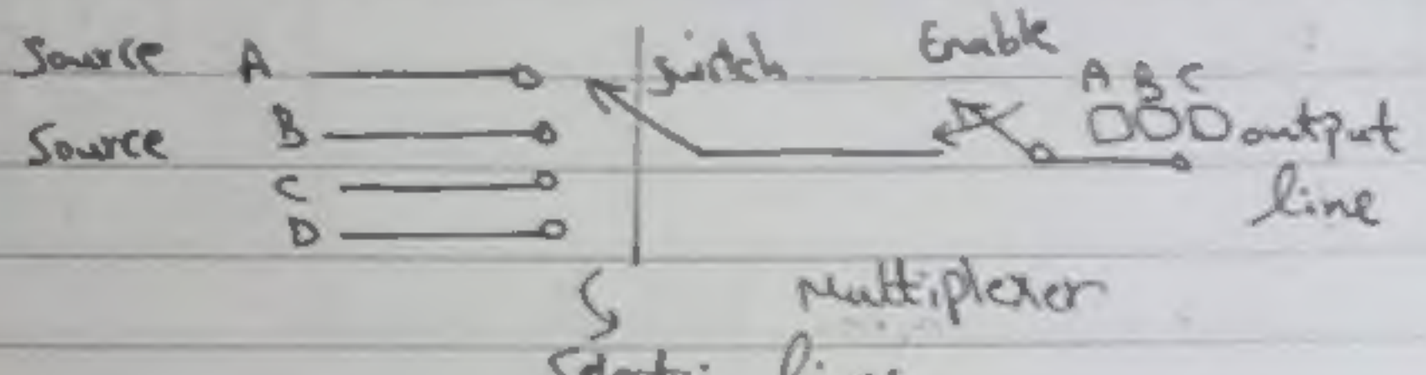
lec (5)
25/10/2016

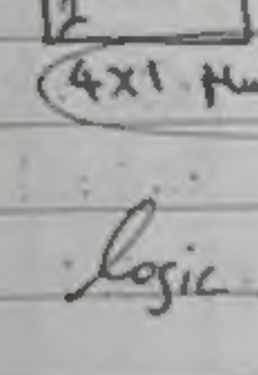
Combinational logic Circuit
"Data processing Circuits"

*Multiplexer



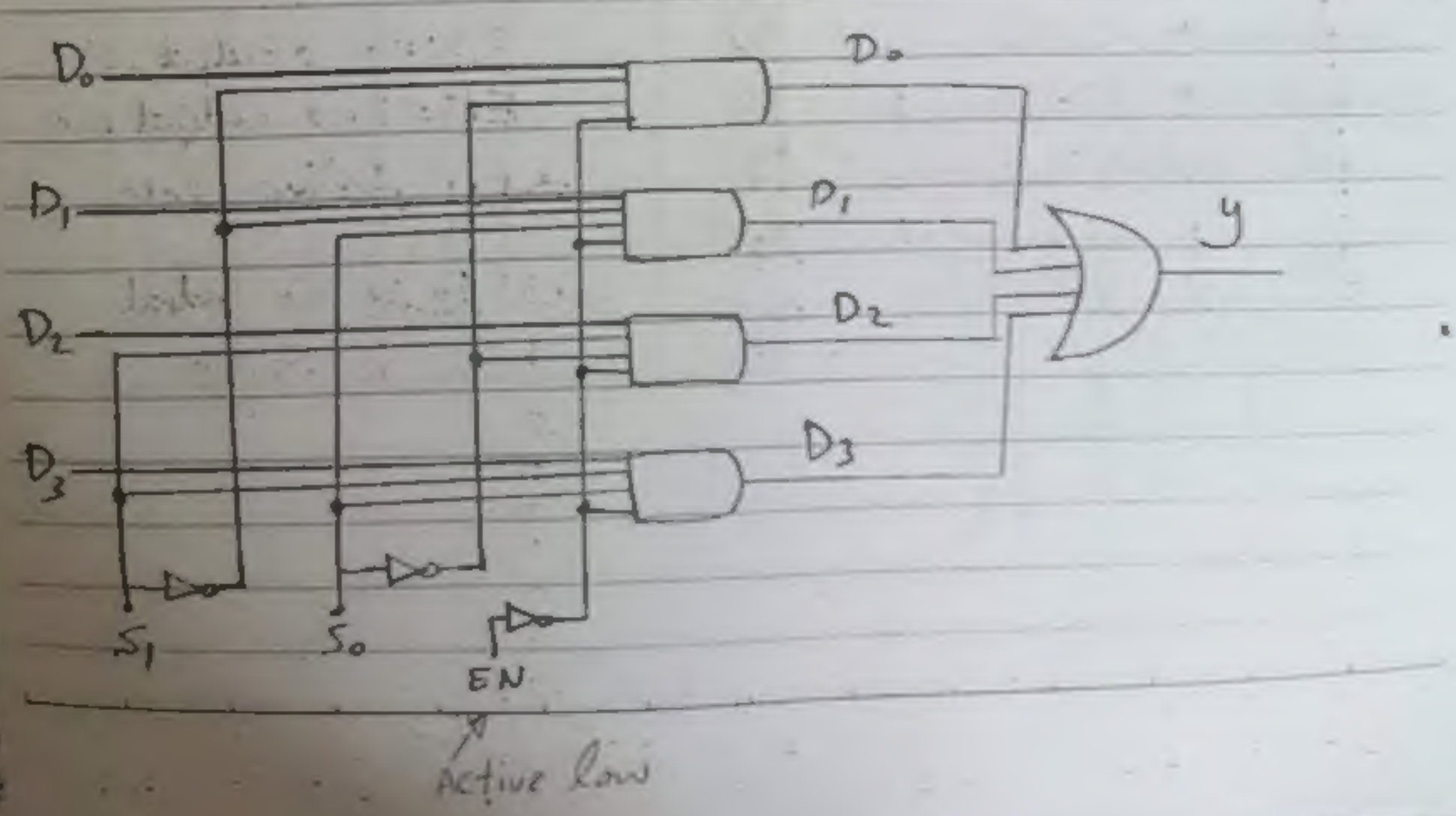
* يستخدم هذا الـ Multiplexer في Time Division Multiplexing (TDM)
* يتكون الـ multiplexer من مجموعة من AND gates.

number of Source $\longrightarrow 2^n \longrightarrow$ output $\longrightarrow 1$



(4x1 multiplexer) ← AND gate يدخل لـ (input) Source كل
(2 selection lines)

Logic Circuit of Mux



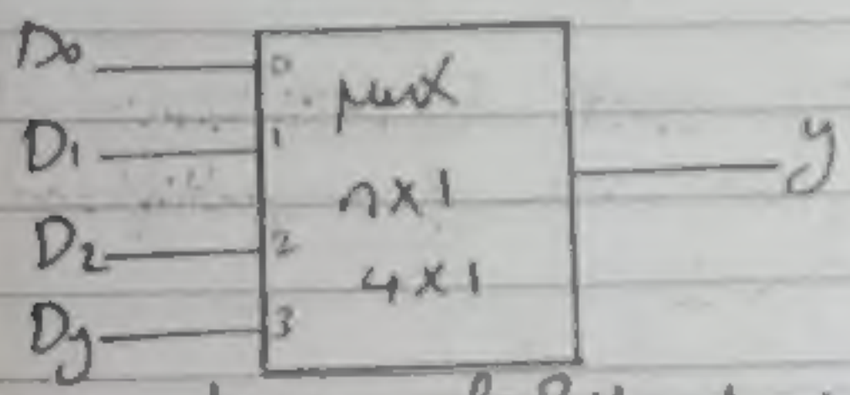
8x1 multiplexer, 3 selection lines

8 → AND gates

* Function table of 4x1 Mux

S_1	S_0	y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

*logic Symbol



* Function table of 8x1 Mux

EN	S_2	S_1	S_0	y
ϕ	0	0	0	D_0
1	0	0	1	D_1
1	0	1	0	D_2
1	0	1	1	D_3
1	1	0	0	D_4
1	1	0	1	D_5
1	1	1	0	D_6
1	1	1	1	D_7
0	X	X	X	0

EN = 0 → output = 0

EN = 1 → output = 1

* EN Active high

EN = 0 → output = 1

EN = 1 → output = 0

*EN Active low

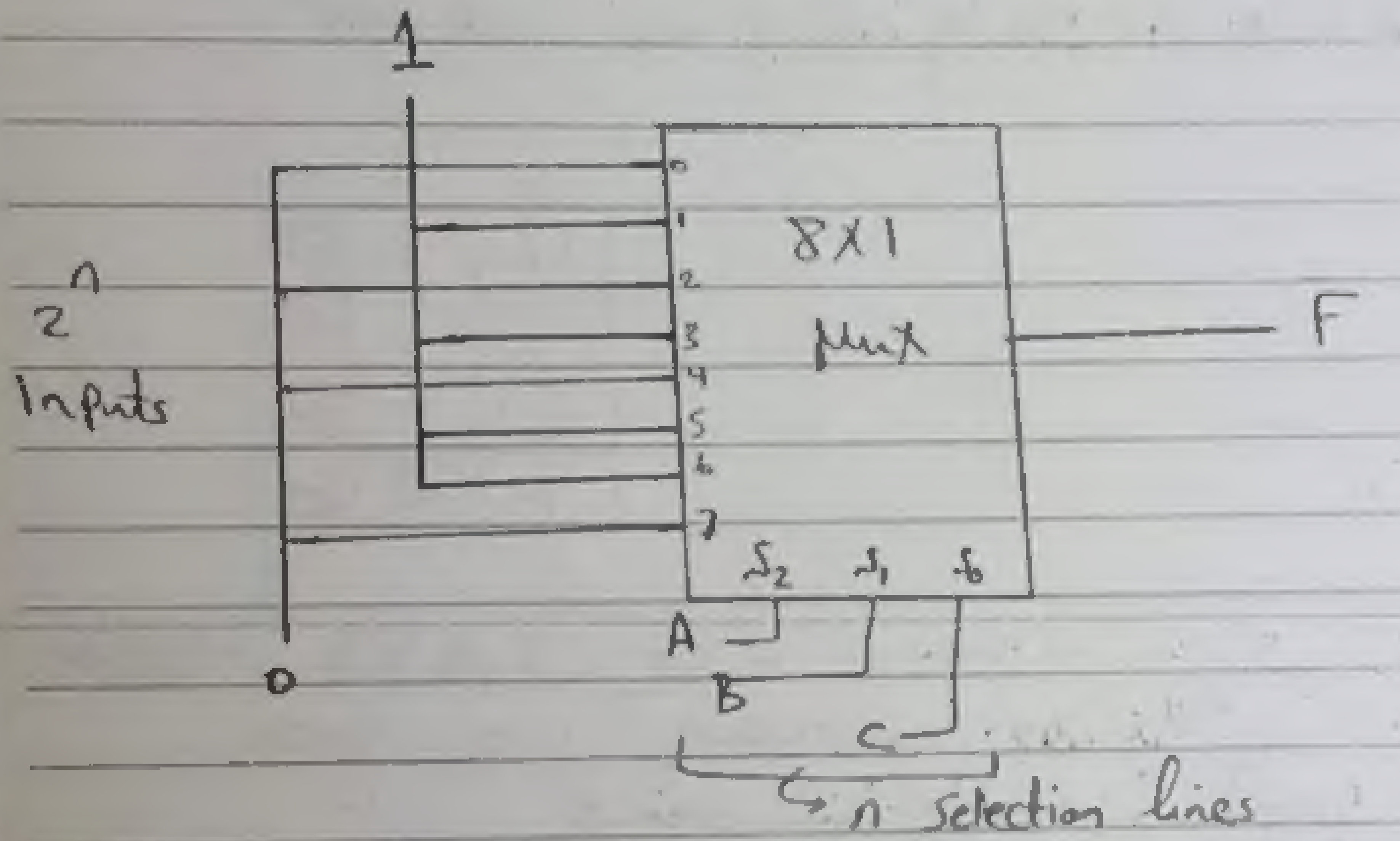
EN	S_2	S_1	S_0	output
1	X	X	X	0
0				
0				
0				
0				

→ Sum of product

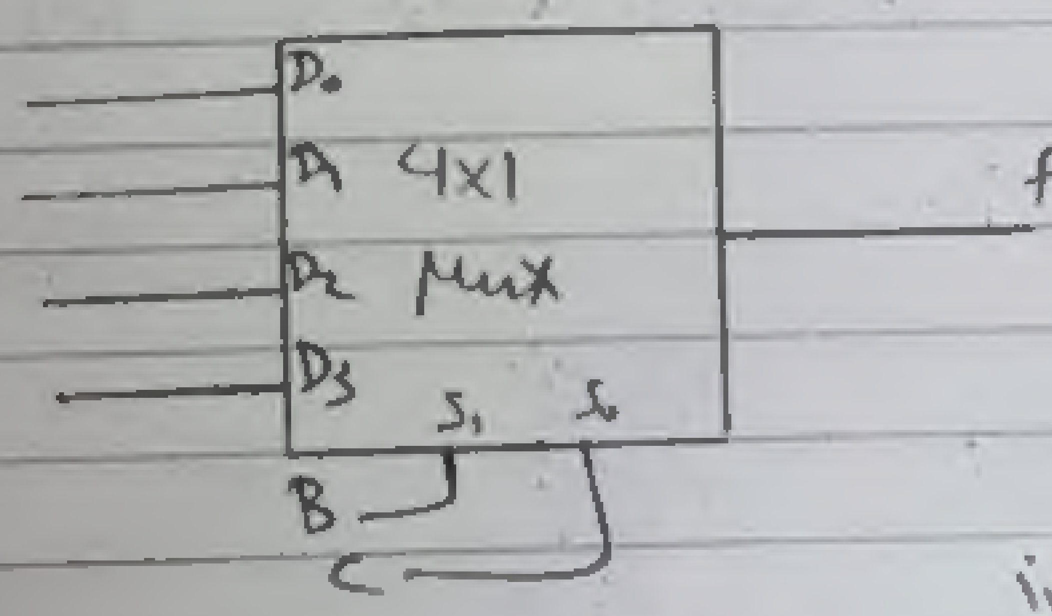
* $F(A,B,C) = \sum m(1,3,5,6)$ القيم اللي عندها F بواحد.
↳ minterm

Implement F using 8:1 multiplexer.

$F(A,B,C) = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + AB\bar{C}$ → من truth table



* Implement the previous Function using 4X1 mux.
← هنا فدا اي selection تم input ل mux لان n المطلوب يساوي 2 فقط.



$F = \sum m(1,3,5,6)$

④ طريقة تحديد inputs
① نضع دائرة ع الارقام المقابلة minterms
② ال inputs اللي هنعد ش دوائر ← صفر والي عنده ← واحد.

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الدائرة الى تمام A ← A
الدائرة الى تمام $\bar{A}$ ← $\bar{A}$

	D_0	D_1	D_2	D_3
$\bar{A}$	0	①	2	③
A	4	⑤	⑥	7
	0	1	A	$\bar{A}$

* طريقه أخرى باستخدام Selection ⇐ A,B

	$\bar{C}$	C
D_0	0	①
D_1	2	③
D_2	4	⑤
D_3	⑥	7

ملاحظه $F(A,B,C,D) = \cdots\cdots$
using 8×1 multiplexer
B, C, D → selection lines
A ⇒ نفس الطريقه السابقه
أو طريقه أخرى باستخدام function table multiplexer

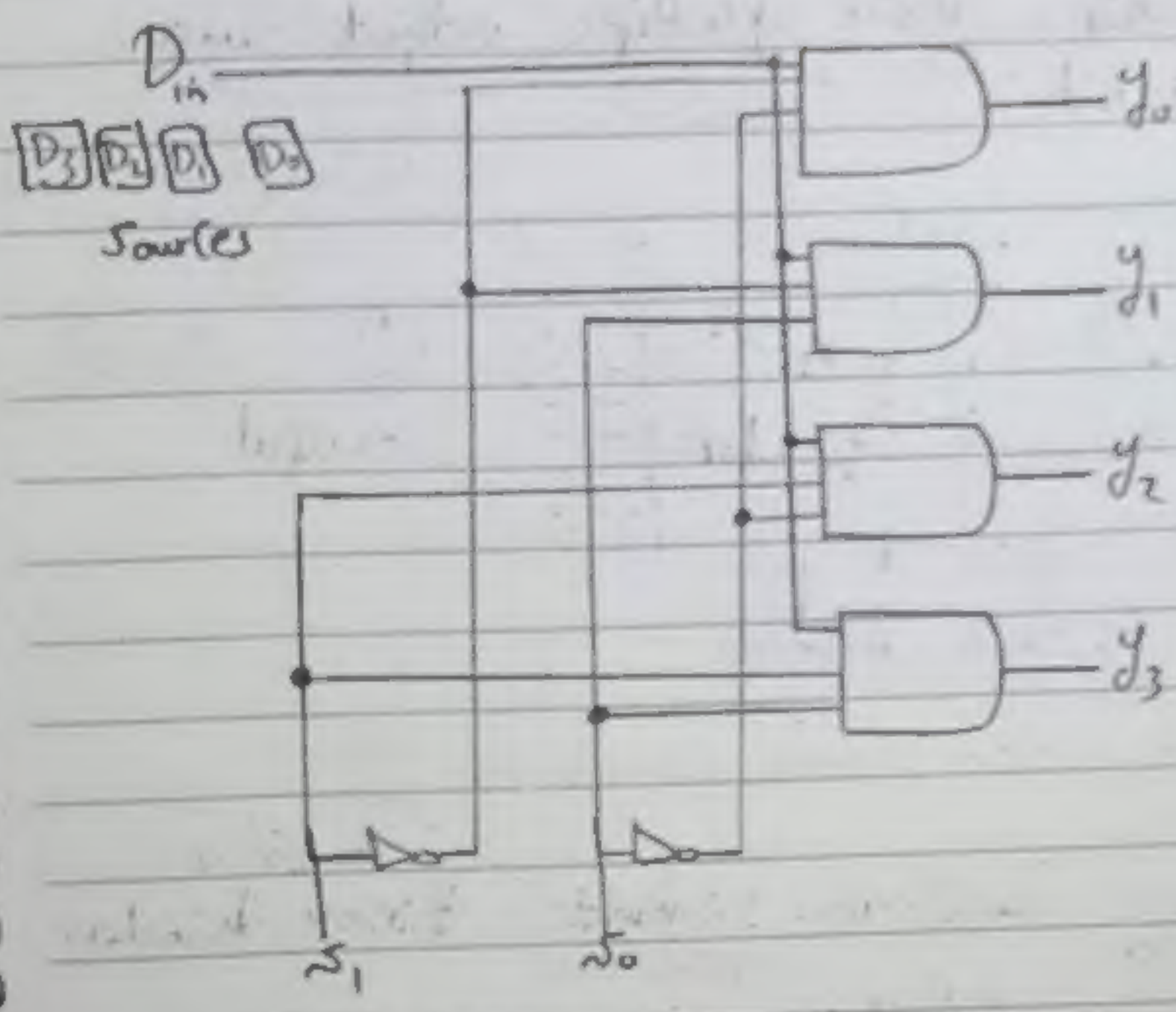
74××151 → (8×1 mux)

* Demultiplexer:-

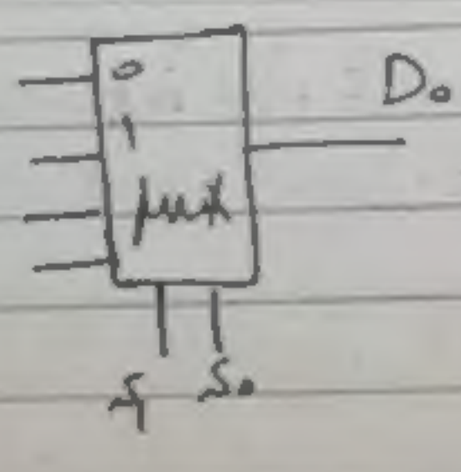
1 line/input
000

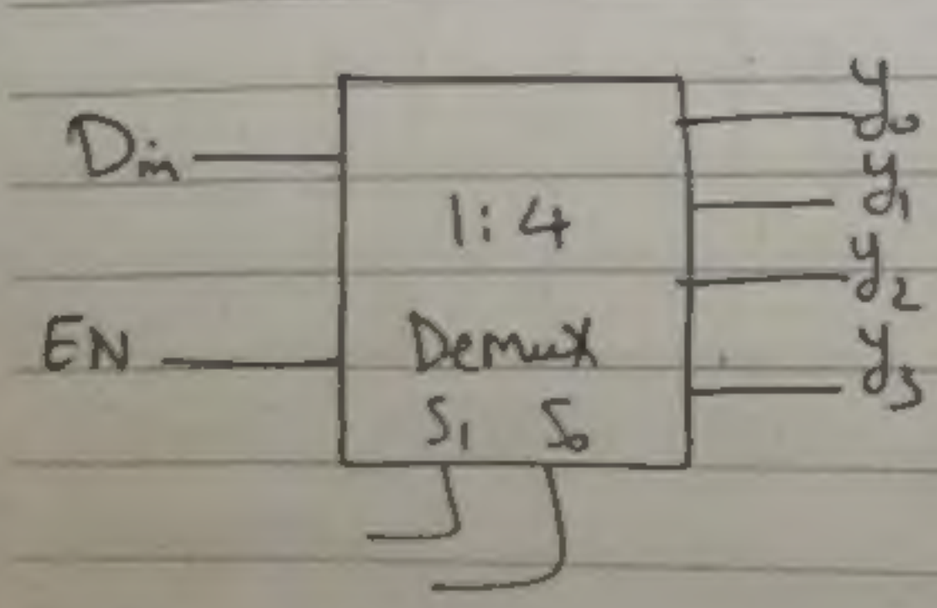
D_0 0
D_1 1
D_2 2
D_3 2^n

* Logic Circuit of 1X4 Demux

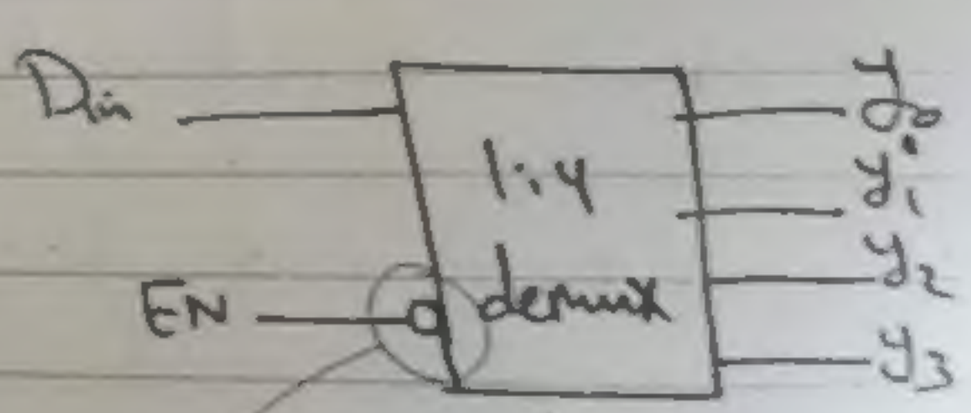


* Symbol





EN → Active high



EN → Active low

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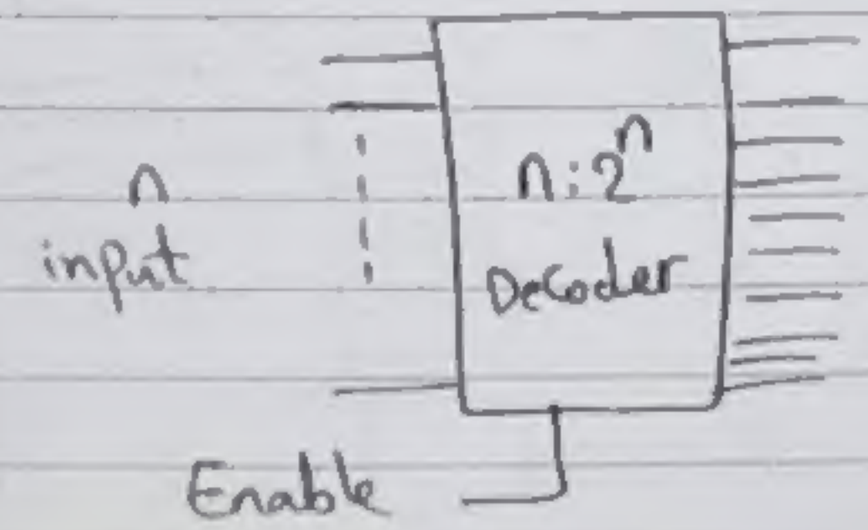
* Mux → Multiple input , Single output logic Circuit.

* Decoders Multiple input , Multiple output logic Circuit

تستعيز الداتا وبيسفرم
في
Security



ABC → 0000 0000
000

* انواعه :-
2 Seven Sigment 2 Binary decoder
2 octal decoder

* ملاحظه معنى Selection lines .

⊛ Function table of Decoders (2:4 line decoder)
(Active high Decoder).

A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Circuit Diagram ← AND gate يتكون من

Code word
01 → 0100
10 → 0010
11 → 0001

Active low ——uses——→ NAND gate in Circuit diagram.

* octal Decoder
3:8 line Decoder (8 AND gate لگتا ہے)